**Lab 9**

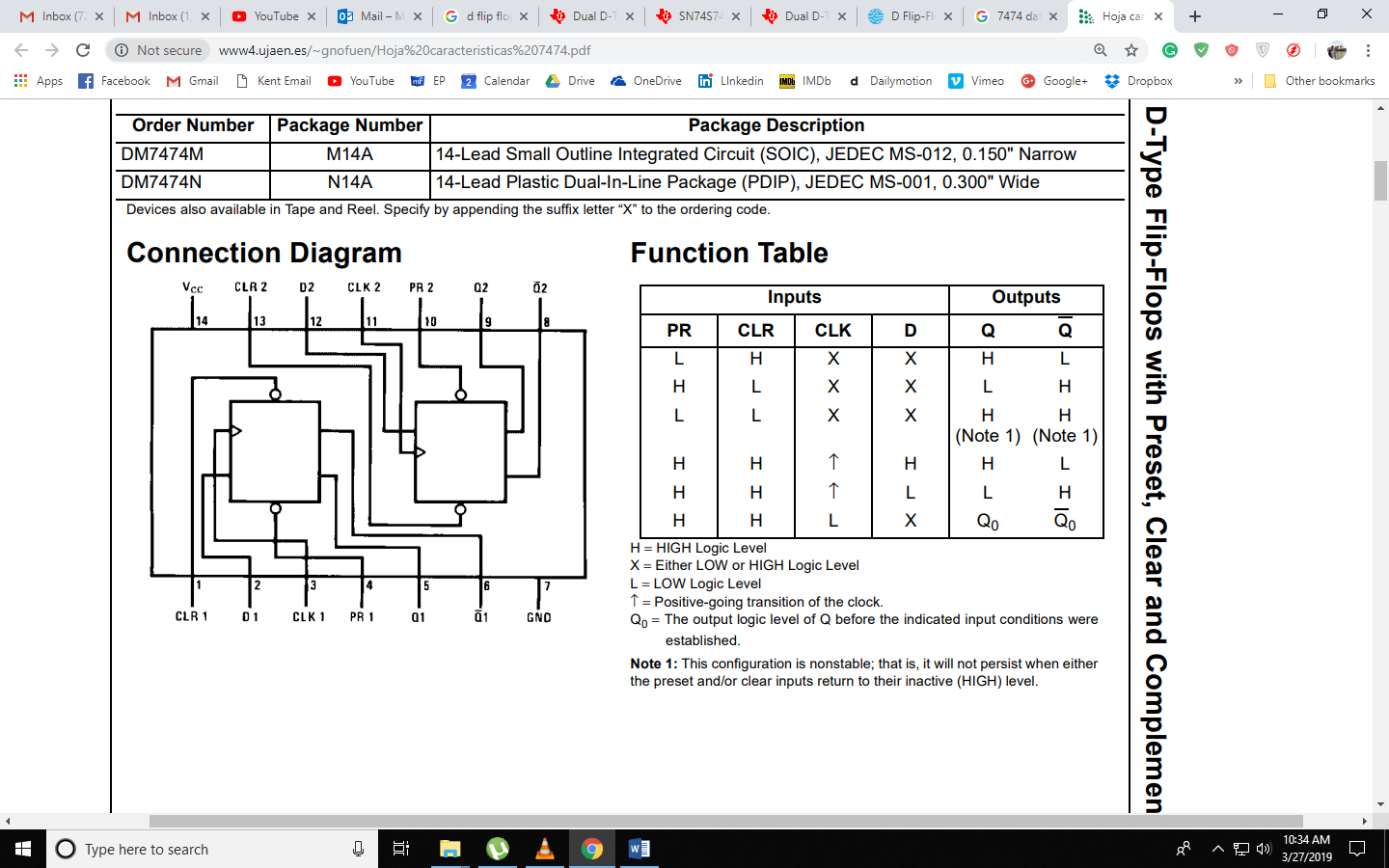
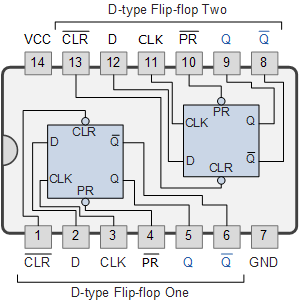
## Objectives:

To learn and understand the working of Flip-Flops and Latches

## Flip-Flop

A flip-flop is a memory device that samples and acts upon its input lines only when it is told to do so with a special timing signal called the clock. This may be in the form of a level or an edge. The student should understand how a latch or flip-flop works to hold the data set and reset states.

### D-Type Flip-Flop

This device contains two independent positive-edge-triggered D-type flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. LOW logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs. 

**JK Flip-Flop**

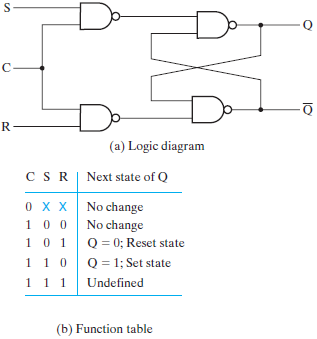
This device contains two independent negative-edge-triggered JK-type flip-flops with complementary outputs. The information on the J and K is accepted by the flip-flops on the negative going edge of the clock pulse. LOW logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

|  |  |
| --- | --- |
| Image result for SN7476 |  |

**Lab Tasks:**

**Question 1**

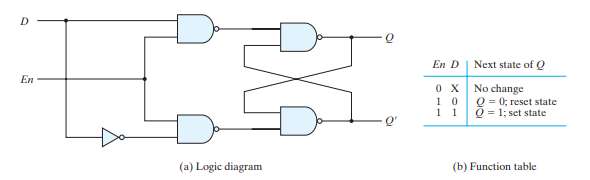
Implement an SR latch with control input as follows:



**Question 2:**

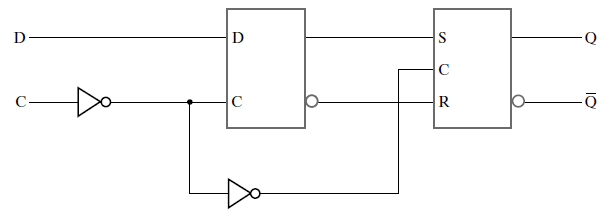
The D latch of Fig below is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a D latch. In each case, draw the logic diagram and verify the circuit operation.

1. Use NOR gates for the SR latch part and AND gates for the other two. An inverter may be needed.
2. Use NOR gates for all four gates. Inverters may be needed.
3. Use four NAND gates only (without an inverter).



**Question 3 (Hardware):**

Design a positive-edge triggered Master-Slave D-type flip-flop.



**Question 4:**

For the sequential circuits given below

1. Write flip-flop input equations
2. Write output equation
3. Derive state table
4. Draw state diagram
5. Implement it on trainer and verify output with help of state table and state diagram

